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# A Novell High-speed low-power domino logic technique for static output in evaluation phase for high frequency inputs

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***Abstract*— Domino logic is widely used for high switching speed and high performance circuits. In dynamic logic, problem arises while cascading one gate to another. In order to cascade dynamic logic, domino logic is used which consists of an inverter used between two stages. Robustness of domino logic diminishes with downscaling as leakage power increases. This paper presents a new proposed domino logic circuit with improved speed. Present work proposed domino logic scheme which gives static output also in evaluation phase with high frequency inputs which other domino techniques do not support. This proposed circuit is designed by making use of modified keeper circuitry. The proposed circuit has low power- delay product as compared to other domino logic circuits. All the circuits have been simulated in cadence virtuoso 180nm technology. According to simulations, the circuit shows much better performance as compared to conventional domino logic circuits.**

***Keywords*— Domino logic; dynamic gates; evaluation phase; pre-charge phase; static gates.***

## I. INTRODUCTION

CMOS gates are basically designed using static logic and dynamic logic. Static logic gates comprises of both pull-up network and pull-down network. This leads to some problems like area requirement for the circuit design is more and also short circuit power consumption is increased as a result of contention between pull-up network (PUN) and pull-down network (PDN) during the transitions of the gate inputs, especially for large fan-in gates. The number of transistors required for N-input gate is 2N. Pseudo-NMOS logic overcomes these drawbacks. Pseudo-NMOS comprises of a grounded PMOS transistor in PUN and PDN performs the evaluation function. Pseudo-NMOS logic is 5 times faster than static CMOS. Also, the numbers of transistors required for N input gate reduces to N+1.This leads to reduced area requirement for the design. But this leads to increase in static power consumption as the grounded-PMOS used in pseudo-NMOS conducts at all times even if PDN is turned OFF. By combining the advantages of low power consumption of static CMOS and reduced area requirement for Pseudo-NMOS logic, dynamic logic circuits designed by introducing clock in the circuit. In dynamic gates, the PDN performs the logic function while PUN is a single PMOS which is driven by clock. Dynamic logic leads to requirement of N+2 numbers of transistors for a gate of fan-in N. There are two major phases of dynamic circuit operation: pre-charge phase and evaluation phase. In pre-charge phase, dynamic node charges through PUN and in evaluation phase, it either remains charged or discharged based on the logic performed by evaluation network [1]. Problem arises while cascading the dynamic gates. Dynamic logic basically suffers from the problems of charge sharing, charge leakage and capacitive coupling etc [2].

To overcome this problem in cascading of dynamic gates, Domino logic is used which is basically an inverter placed in between the two cascading stages. The domino gates are usually non-inverting because of inverter placed at output node. For reducing the charge leakage problem, keeper circuitry is used in domino logic. Whenever a logic function is performed such that it does not discharge the dynamic node through PDN, keeper circuitry keep the dynamic node charged through supply voltage and in this way prevents charge leakage. Domino logic is used for high-speed applications such as data-path in microprocessor [3].

In order to increase robustness, the best way is to upsize the keeper circuit [4]. The keeper is need to be strong enough to resist noise, leakage etc. Also, it should be chosen such that to allow the evaluate node discharge quickly when it is supposed to discharge and keeper strength should be relatively weak for low supply voltages in order to reduce contention with pull-down stack(s).Among all domino techniques high-speed domino logic[5] and conditional keeper domino logic[6] provides the most robust outputs. They make use of delayed version of clock to improve robustness. All the conventional domino logic techniques does not allow the charging of dynamic node again in evaluation phase if it is discharges once until next pre-charge phase comes. Thus circuit does not give correct output if input changes during evaluation phase. In this paper, we propose a domino technique which gives static

output in evaluation phase for high frequency inputs. This is done by modifying the keeper circuit, using footer transistor for preventing charge leakage during pre-charge phase and by using modified level restorer circuit for leakage reduction while maintaining the same current capability. The proposed circuit offers less power dissipation and better power-delay product.

## II. PREVIOUS WORK

The dynamic node is floating in evaluation, so it is susceptible to noise which may lead to distorted output. Noise sources may be glitches and current leakage etc. So the dynamic node should be made stable in order to give correct output.

The typical domino logic style includes footless domino logic[7], footer domino logic[8], high speed domino logic, conditional keeper logic etc. Fig. 1 shows the circuit for AND gate in static CMOS logic as well as in domino logic. Simply the area requirement for designing AND gate by using CMOS logic and domino logic can be seen. Here, keeper transistor is used for preventing charge leakage and providing better performance.

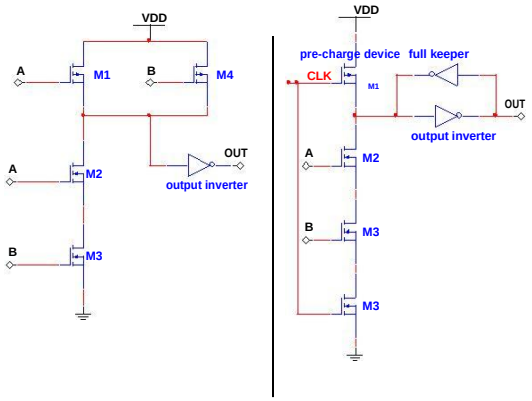


Fig.1 Implementation of AND gate using (i) static CMOS logic (ii) NMOS domino logic.

Fig.2 shows the (a) footer domino logic style (b) footless domino logic style for high fan-in OR gate implementation. The footer domino style has less power dissipation as compared to footless domino style because of stacking effect. In case of footer domino logic style, a footer transistor is used below evaluation network as shown in Fig II (a) which is operated by the clock. When clock goes high in evaluation phase only then footer transistor switches ON and provides a discharge path according to logic function performed by the evaluation network otherwise it turns OFF in pre-charge phase so reduces the leakage [9] hence the power dissipation. In case of footless domino style, there is no footer transistor which leads to more power dissipation.

As technology is scaled down, leakage is increased and robustness of circuit decreases. As if high fan-in gates are used, leakage is more because of number of transistors increases which leads to discharge the dynamic node and leads to incorrect output. Also the charge sharing, glitches lead to faulty output. So in order to prevent this leakage, keeper circuit is used which keep the dynamic node charged to logic HIGH even if there is no discharge path through the evaluation network.

The use of keeper provides immunity from noise and leads to correct output. The simplest way to enhance robustness is to increase the size of keeper transistor but this leads to contention between keeper circuit and PDN and results in increased delay and power dissipation of the circuit. Also to upsize the keeper (increase width) leads to more static power dissipation because noise at any inputs lead to direct path for current from VDD to ground through keeper transistor. Therefore there is trade-off between keeper circuit width and power and delay. This makes the network slower and more dissipating. So, for high speed applications, weaker keeper circuit is used and for highly robust circuits, stronger keeper is used. However FDL style reduces the leakage and power dissipation considerably but delay is also increased.

The keeper ratio is defined as

$$K = \frac{\beta p(W/L)keeper}{\beta n(W/L)evaluation\ network - transistor}$$

where W and L shows transistor size and $\mu_n$ and $\mu_p$ are electron and hole mobility respectively.

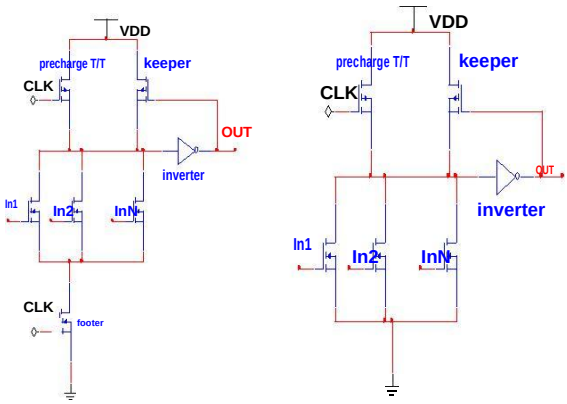


Fig. 2 Implementation of high fan-in OR gates using (a) footer domino logic (b) footless domino logic.

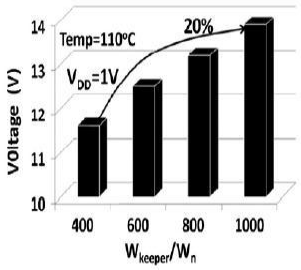


Fig.3 Keeper sizing effect on power dissipation for 32-input OR footless domino logic (FLDL).

Here $W_{keeper}$ denotes width of keeper and $W_n$ denotes width of pull-down network device.

2.1 High Speed Domino Logic

Here delay is introduced in clock by using two inverters as shown in Fig.4, in order to reduce the current through the PMOS keeper at the starting of evaluation phase which leads to reduce the power dissipation up to some extent. This makes it possible to use strong keeper without performance degradation and improve the noise margin. But the power and area overhead of clock delay circuit remains. In pre-charge phase, when clock becomes LOW, transistor $M_{p1}$ turns ON and dynamic node is charged to logic HIGH and in the beginning of evaluation phase, $M_{p2}$ still turns ON which keeps the keeper transistor $M_k$ to OFF condition.

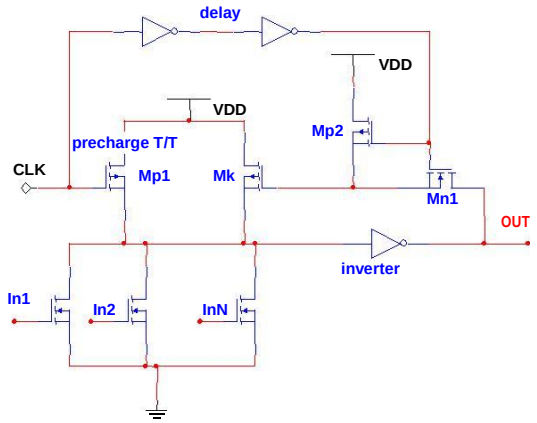


Fig.4 High speed domino logic [5]

After delay completion $M_{p2}$ turns OFF. In between this, the inputs perform the logic function and in case if input(s) are logic HIGH then provides discharge path for dynamic node and output changes to logic HIGH and $M_k$ is in OFF condition as a logic high as ($V_{DD}$-$V_{tn}$) voltage, where $V_{tn}$ is NMOS threshold voltage, is passed to $M_k$ which does not turn it into ON state. And if no input is HIGH then dynamic node is not discharged and output is still LOW. So $M_{n1}$ turns ON and pass logic LOW to $M_k$ which turns it ON and dynamic node is kept at logic HIGH. In this way, keeper transistor prevents charge leakage in High speed domino logic.

The problem with high speed domino logic[4] (HSDL) is that a voltage of $V_{DD}$ - $V_{tn}$ is passed through the NMOS transistor $M_{n1}$ which leads to a small dc current through the keeper transistor and pull-down network and also large noise at input terminals of PDN causes the dynamic node discharge because of no footer transistor.

2.2 Conditional Keeper Domino Logic

It is also one of the standard versions of domino logic as shown in Fig.5. Here two keeper transistors are used. At the beginning of evaluation phase, the smaller keeper K2 charges the dynamic node in case if all the inputs are LOW. Then after delay completion, if dynamic node still remains charged, the NAND gate turns the larger keeper transistor ON to keep the dynamic node HIGH for the rest of evaluation phase. If the dynamic node has discharged, the keeper transistors remain OFF. This circuit has some drawbacks such as decreasing delay of the inverters and the NAND gate has some limitations.

Robustness [11] can be achieved by using the larger keeper. The increase in size of delay element improves noise immunity [12] but power dissipation and delay increases.

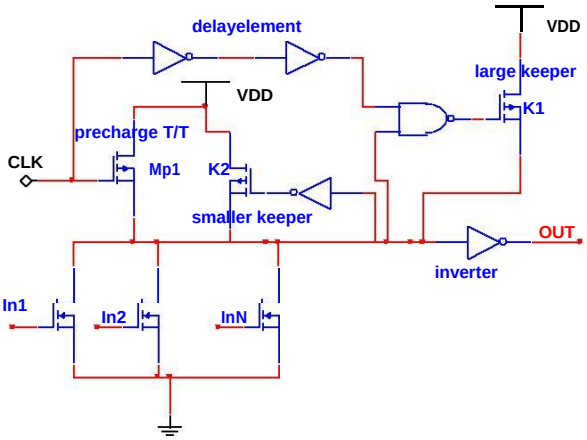


Fig.5 Conditional keeper domino logic [6]

## III. PROPOSED LOGIC STYLE

W e have proposed logic style that makes use of level restorer circuit, modified keeper circuit, stacking effect and better performance results are obtained as compared to standard domino logic styles. All the simulations have been done on cadence virtuoso 180 nm technology.

1) Level restorer circuit

We use ULPD based level restorer studied in [14] .ULPD is ultra low power design. There can be various designs of ULPD which are shown in fig.6

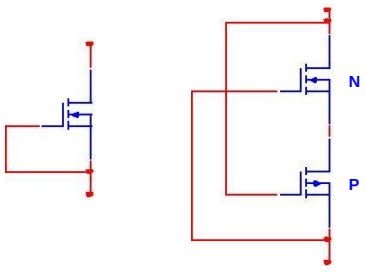


Fig.6 ULPD based level restorer

It maintains same current capability while reduces the current leakage as compared to standard diode. ULP leakage is obtained because when the ULPD is reverse biased, both

transistors operate with negative $V_{gs}$ voltages, leading to strongly reduced leakage current in comparison to standard diodes. When reverse bias is increased further current through ULPD increases firstly up to peak then decreases abruptly because of more negative $V_{gs}$ of the transistors.

By making use of ULPD and some other techniques, circuit is designed which gives static output in evaluation phase for high frequency changing inputs as shown in Fig.7. In this circuit we make use of delayed clock. The keeper circuit is modified as well. The inverter I1 used at dynamic node is made with low threshold NMOS such that it turns ON when a very small voltage applied to it. Two inverters are placed for introducing delay in CLK so that in the beginning of evaluation phase, the footer Mn1 is OFF. During this period, evaluation network performs the operation. Transistor Mn4 used is of high threshold voltage. It only turns ON when output is strong. It prevents further discharge from Mn2. Transistor Mn2 used is also having high threshold value. Transistors Mn6 and Mn7 are used for improving the circuit by leakage reduction [15] also lead to reduction of delay and power dissipation.

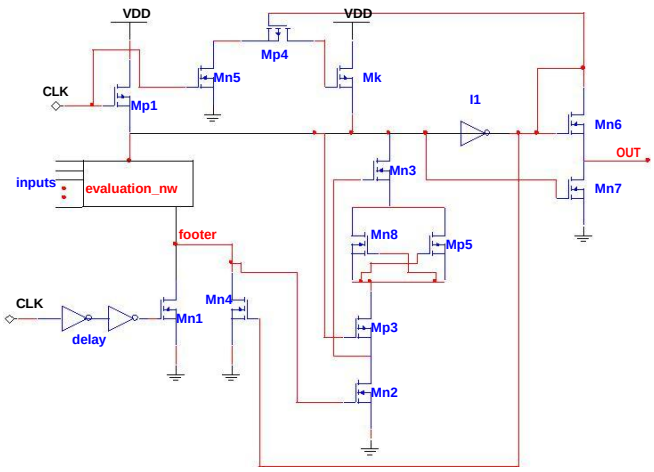


Fig.7 Proposed Domino logic style

In pre-charge phase, when clock is low, dynamic node charges through pre-charge transistor Mp1 and transistor Mn5 is in OFF state. In the beginning of pre-charge footer transistor is ON because of delay and it may lead to discharge dynamic node but as pre-charge phase is going on, dynamic node still remains HIGH.

When CLK becomes HIGH, evaluation phase begins. In the beginning, the footer transistor Mn1 is in OFF state because of delay introduced. In this time slot, evaluation network performs its logic function. If any input combination tries to pull the dynamic node down, the transistor Mn2 is turned ON and the dynamic node is discharged through the transistors Mn3 and Mp3. This whole circuitry is preventing leakage in the beginning of evaluation phase by making use of stacking effect. After delay completion, Mn1 turns ON and provides the rest discharging path and Mn2 is turned OFF. In case if no input makes discharging path, we have to make sure that the voltage at footer node should not turn ON the transistor Mn2 so Mn2 is chosen of high threshold value. As dynamic node is charged so we get logic LOW at output, which turns ON Mp4 and Mn5 is also turned high as CLK is high, so keeper transistor Mk is turned ON to keep the dynamic node charged and prevents charge leakage.

Input makes discharging path, we have to make sure that the voltage at footer node should not turn ON the transistor Mn2 so Mn2 is chosen of high threshold value. As dynamic node is charged so we get logic LOW at output, which turns ON Mp4 and Mn5 is also turned high as CLK is high, so keeper transistor Mk is turned ON to keep the dynamic node charged and prevents charge leakage.

Now consider the case, if dynamic node is discharged and any input changes (from high to low), as dynamic node is floating condition now, so we designed the inverter I1 such that it turns ON even with very small input to it as mentioned earlier. So output turns to low which turns ON the transistor Mp4 which provides the strong LOW logic to keeper Mk through Mn5 and dynamic node is charged again. Further charging and discharging happens in same manner.

In this way, proposed circuit is capable of providing static output in evaluation phase with input changing at high frequency.

## IV. SIMULATION RESULTS

We simulated different topologies using cadence virtuoso 180nm technology models. And we took 32 fan-in OR gate as evaluation network for all topologies. The simulation results are tabulated here.

To compare different topologies, we use power consumption, delay and power-delay product (PDP).

TABLE 1. Comparative performance for different standard and proposed topologies

| Parameters | Topologies | | | | |
|---|---|---|---|---|---|
| | Footless | Footer | HSDL | CKL | PROPOSED |
| **Power Dissipation ($\times 10^{-5}$ W)** | 6.2 | 4.5 | 6.1 | 6.2 | 1.2 |
| **Delay($\times 10^{-9}$)** | 1.02 | 2.06 | 0.61 | 0.72 | .35 |
| **PDP($\times 10^{-14}$ J)** | 6.32 | 9.27 | 3.721 | 4.464 | .42 |

It can be seen that proposed design shows significant improvement in performance. Table 1 shows the different values of power, delay and PDP at $V_{DD}$=1.5 V.

Delay of circuit is reduced as we are using separate path for discharging. The leakage current is reduced by the introduction of stacking effect.

The outputs of footer domino style, footless domino style, high speed domino style and proposed domino circuit are shown further.

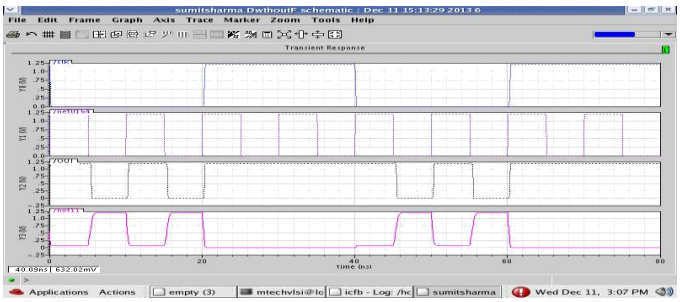

Fig. 8 Output wave form of footless domino style

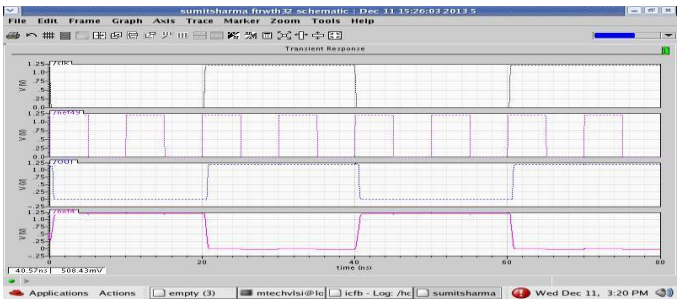

Fig. 9 Output wave form of footer domino style

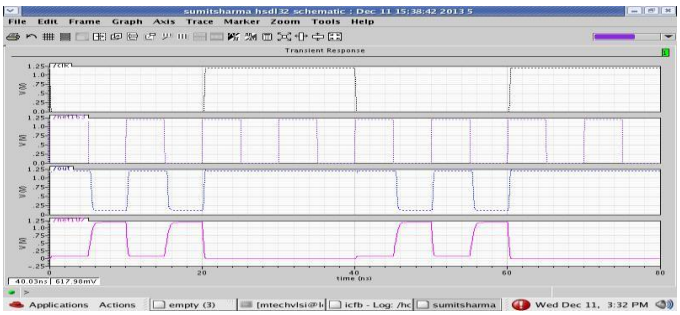

Fig. 10 Output wave form of high speed domino logic

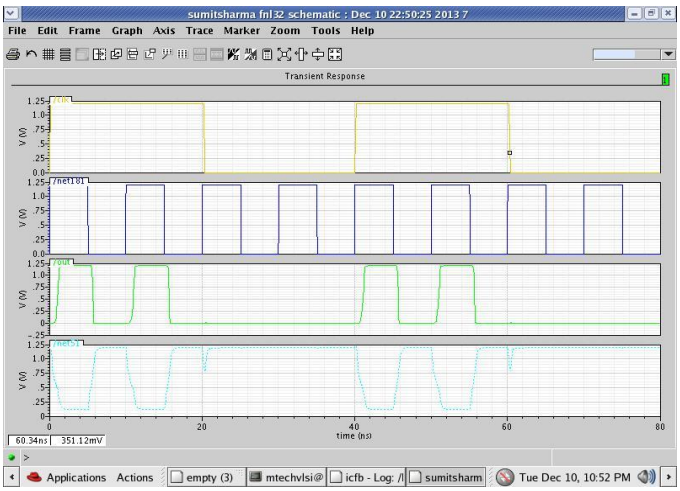

Fig. 10 Output wave form of high speed domino logic

These outputs are taken by using 32 fan-in OR gate as evaluation network. The proposed circuit has more area as number of transistors is increased.

## V. CONCLUSIONS

In this paper, we proposed new domino logic style that gives static output in evaluation phase for high frequency inputs. It also shows better performance compared to other conventional domino logic families. But this circuit is not totally free from glitch power dissipation at its output so further some improvement is required.

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